On The Design of High Perfprmance Reconfigurable DSP processor using FPGA

Saurav Mandal, Ashis Kumar Mal

Abstract— In this paper, a high performance reconfigurable combined architecture of Discrete Wavelet Transform (DWT), Matrix Multiplication and Fast Fourier Transform is presented. This reduces area and become cost-effective. In the proposed DWT architecture the input data are separated as even and odd numbers of data as well as both data are inputted parallel. This cause faster DWT operation then conventional architecture. In conventional architecture N-point DWT is computed in N cycles where proposed architecture N-sample sequence is computed in only N/2 cycles. Therefore they are at least twice as fast as the conventional architecture. On this paper we have proposed the parallel based reconfigurable Matrix Multiplication architecture as well as the pipeline reconfigurable Fast Fourier Transform architecture which increase the speed of computation. This paper also presented a novel reconfigurable architecture for implementing DSP algorithms.

Finally we showed the mat lab simulation result of the proposed FFT architecture and Matrix Multiplication simulation result verified using mentor graphics tool. The proposed three architectures are synthesis using XILINX ISE 9.1i version and the results have been presented.

Index Terms— Discrete Wavelet Transform, Matrix Multiplication, Fast Fourier Transform, Processing Elements,Switch Matrix, Random Access Memory,Very large scale integration circuits

.

1 INTRODUCTION

In recent years, DWT become a popular tool for many signal and image processing application. This is because it has features such as progressive image transmission by quality image resolution and ease of compressed image manipulation .The demand of low power VLSI circuit in modern wireless communication systems is all the time growing. On the other hand, advances in the VLSI technology have reduced the cost of hardware. Therefore, the possibility of reducing period, even at the cost of increasing the hardware is becoming an important issue. In fact, low period devices are important also for low-power utilization.

The above consideration has motivated the work of this paper which shortly process scalable architecture having a AT^2parameter which is approximately ½ of that of already existing devices and the proposed DWT architecture which can compute N-sample sequence in N/2 cycle as well as this is parallel base architecture approach for faster operation.

Matrix Multiplication is one of the most fundamental and important problems in science and engineering. Many other important matrix problems can be solved via Matrix Multiplication, e.g. finding n_{th} power, the inverse, the determinant, Eigen values etc. Many graph problem are also reduced by Matrix Multiplication .

- *Saurav Mandal Assistant Professor in DIATM Durgapur, India, PH-09804770559. E-mail: saurav.technology@yahoo.com*
- *Dr. Ashis Kumar Mal Associate Professor in NIT Durgapur, India, PH-0343-2754389. E-mail: akmal@ece.nitdgp.ac.in*

So we have required high speed computation. Above consideration we are presented a parallel based Matrix Multiplication architecture which increases the speed of computation.

Fast Fourier Transform (FFT) has thus evolved as an efficient algorithm for computing DFT. It is an important improvement on the Discrete Fourier Transform Algorithm due to the achievement of significantly lower computational complexity. This paper presents a pipeline FFT architecture which is reconfigurable to the size of FFT problem, the clock speed of execution the number of memory module used at each stage.

On the other hand this architecture consists of reconfigurable Processing Element (PE) array and reconfigurable address generator, featuring dynamically reconfigurable capability.

2 CONVENTIONAL DISCRETE WAVELET TRANSFORM

A basic implementation of a 1-D DWT [3] has been done by using the Daubachies wavelet coefficients. Two different output bands are produced by applying two FIR filters on data input samples. A low pass filter produced low frequency data by using h(x) coefficient as well as high pass filter produced high frequency data by using high pass filter coefficient g(x). The conventional DWT [3] consisting of N- tap low pass filter and N-tap high pass filter. Input data are

a(0) a(1) a(2) a(3) ……..a(N)

During one cycle filtering is operated and the filtered values are stored for next octave. Since one input data are filtered during one cycle, the computation period is N.

3 Draw Backs Conventional Discrete Wavelet Transform

From the above discussion we come to the point that--

a. N-points DWT computed in N-cycles.

b. More number of hardware is required.

c. Power utilization is more.

d. Speed is reduced

e. Required more area.

f. Fixed in only one application.

4 Proposed Architectures

Convolution needs only multiplication and addition, we expected the architecture that performed DWT consists of multiplier, adder and some register. On this similarity we separated the filter in two parts, one has even index coefficient and other has odd index coefficient. For simplicity we called it even filter and odd filter respectively. If input samples are even then it filtered by even filter and odd number of samples filtered by odd filter. In octave 1 low pass filtered output stored in register R for computation octave 2.

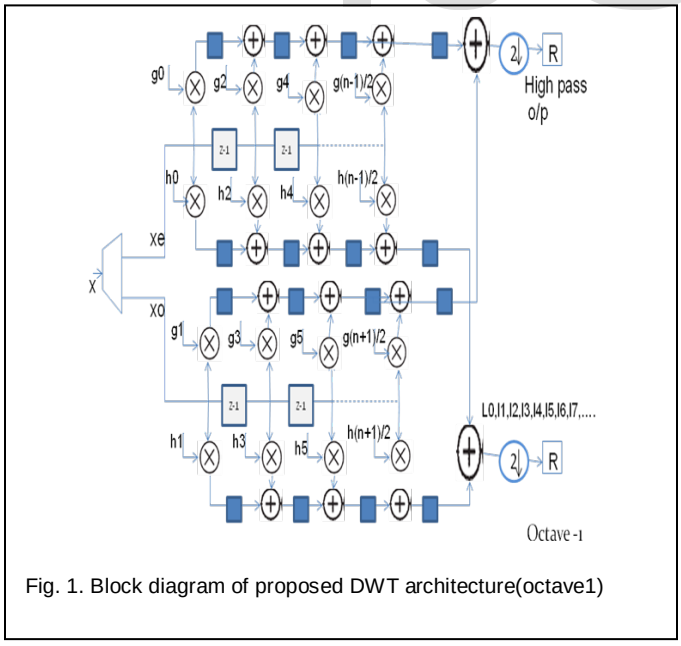

Fig. 1. Block diagram of proposed DWT architecture(octave1)

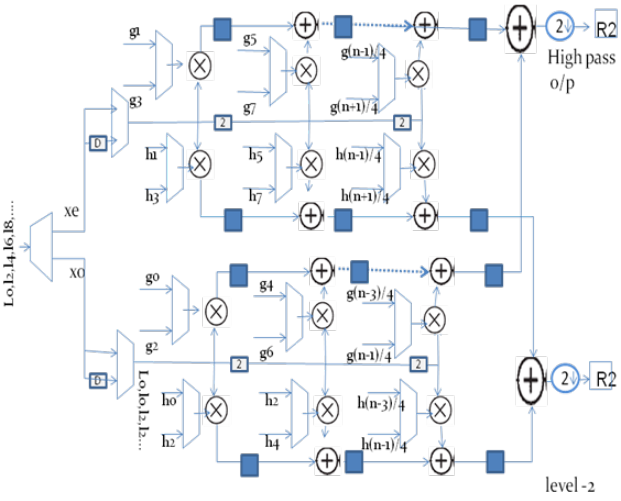

Fig. 2. Block diagram of proposed DWT architecture(octave2)

The input data are divided odd and even no of data. Then odd and even no of data inputted parallel . Let the input data like this.

a(0),a(2),a(4),a(6),……..
a(1),a(3),a(5),a(7),……..

During one cycle, filtering is operated and the filtered values are stored for next octave. Two input data are filtered during one cycle,the computation period is N/2.

In this paper we proposed an architecture that is capable of handling matrices of variable sizes. The hardware suggested incorporates a high degree of parallesim to achive large through put. The design involve a noval approch to multiply two numbers in a single clock cycle. Also parallel approch for fast computation. In this paper also we present reconfigurable processing element, using those processing element we compute any Matrix Multiplication without changing the hardware and algorithm.

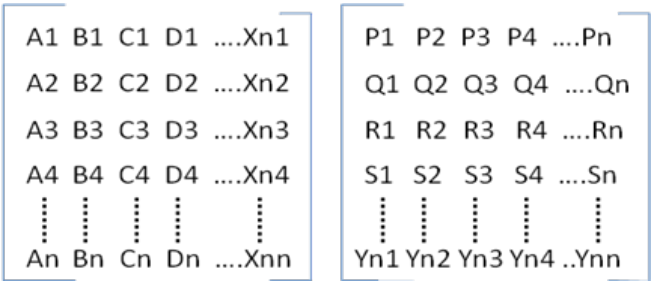

Fig. 3. Block diagram of NXN input matrix

The above figure illustrates two input matrices each of order NXN. Here we are considering only square matrices for explanation purpose. If 2 rectangular matrices are given as inputs, the hard ware checks for the condition of matrix multiplication and continues the work. The hardware for the implementation of multiplication of matrices in figure3 is as given in figure 4.

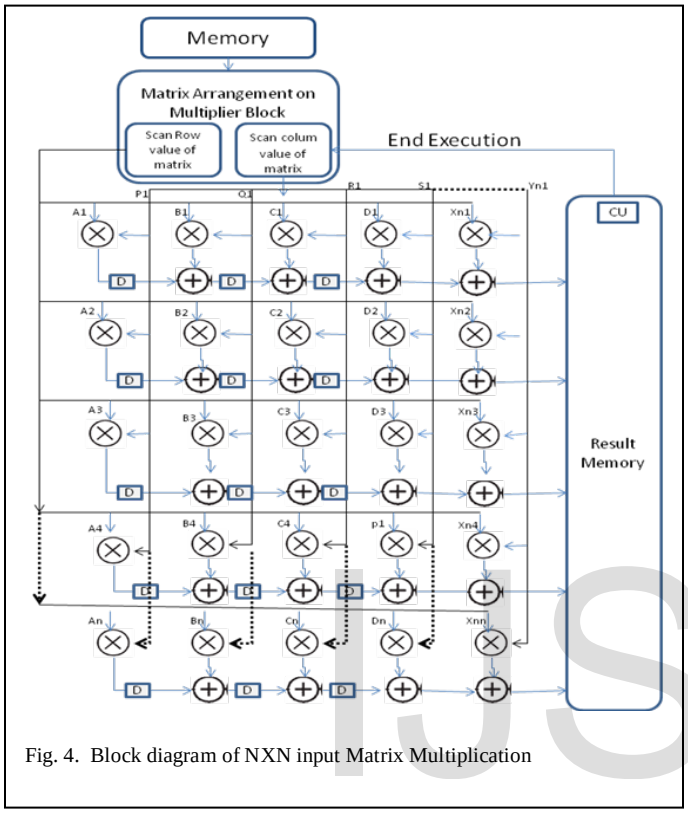

Fig. 4. Block diagram of NXN input Matrix Multiplication

Bit stream for 4x4 Matrix Multiplication.

u= 1 1 1 1 0
v= 1 1 1 1 0
w=1 1 1 1 0
x=1 1 1 1 0

The proposed FFT architecture consists of Processing Elements (PEs). Number of PEs required with respect to FFT computational points. The mathematical representation of decimation-in-time algorithm as follows:

$$X(K)=\sum_{n=0}^{N-1} W^{kn}{}_N$$

$$=\sum_{n=even} X(n)\, W^{kn}{}_N \; +=\sum_{n=odd} X(n)\, W^{kn}{}_N$$

$$= \sum_{m=0}^{N/2-1} X(2m) W^{k2m}{}_N + \sum_{m=0}^{N/2-1} X(2m+1) W^{k(2m+1)}{}_N$$

$W^2{}_N = W_{N/2}$ with this substitution can be expressed as----

$$X(K)= \sum_{m=0}^{N/2-1} f1(m) W^{km}{}_{N/2} + W^k \sum_{m=0}^{N/2-1} f2(m)\, W^{km}{}_{N/2}$$

$$X(k)=F1(k) + W^k{}_N\, F2(k) \quad ,k=0,1,..,N/2-1$$

$$X(k+N/2)=F1(k) - W^k{}_N\, F2(k) \quad , k=0,1,..,N/2-1$$

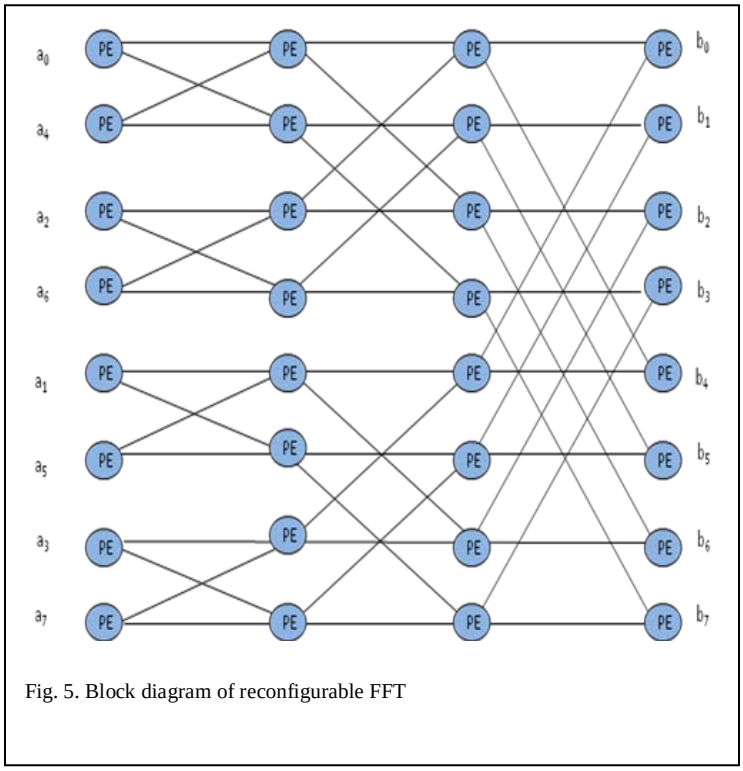

Fig. 5. Block diagram of reconfigurable FFT

The decimation of the data sequence can be repeated again and again until the resulting sequences are reduced to one point sequences. For $N=2^J$, this decimation can be performed $J=\log_2 N$ times. Thus the total complex multiplication is reduced to $N/2 \log_2 N$. Number of complex addition is $N\log_2 N$.

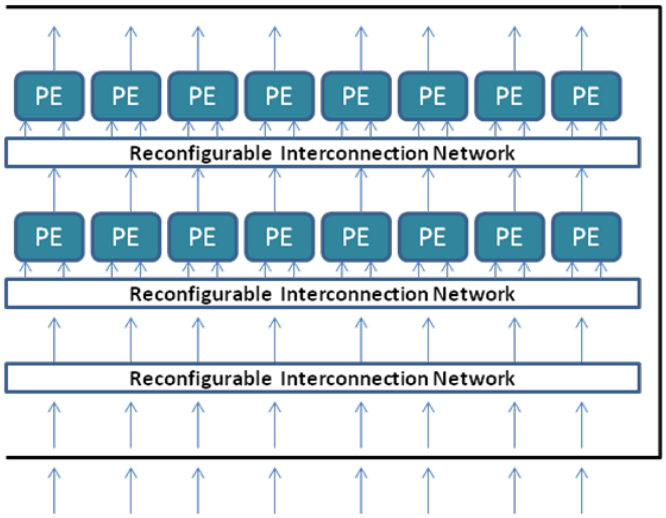

Fig 6. Block diagram of pipeline reconfigurable FFT

While one PEs array is being reconfigured the other array is computing one step of FFT. Reconfigurable interconnection network control the PEs for computing FFT, shown in figure 6
.

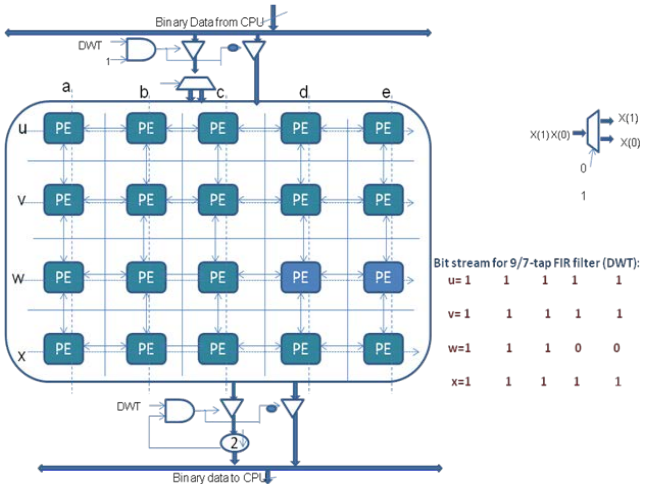

Fig 7. Combined architecture of DWT, Matrix Multiplication and FFT

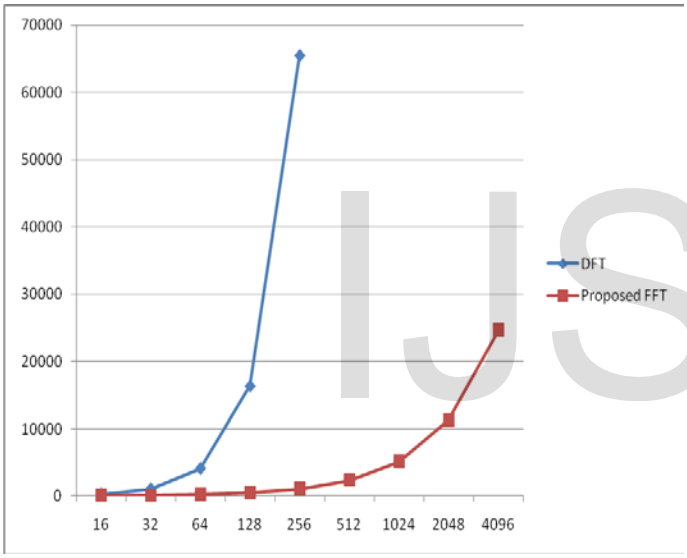

Fig 8.Plot of computational complexity versus no of points

TABLE I. Comparison of Computational Complexity of Two DWT

Number of point	*Direct multiplication by pipeline Architecture* ($N+N/2+N/4+..N/2^{i-1}$)	*Direct Multiplication by Proposed Architecture* ($N/2+N/4+N/8..+N/2^{i}$)	*Speed*
16	30	14	2.14
32	62	30	2.06
64	126	62	2.03
128	254	126	2.01
256	510	254	2.00
512	1022	510	2.00

J=No of stage, $J=\log_2 N$

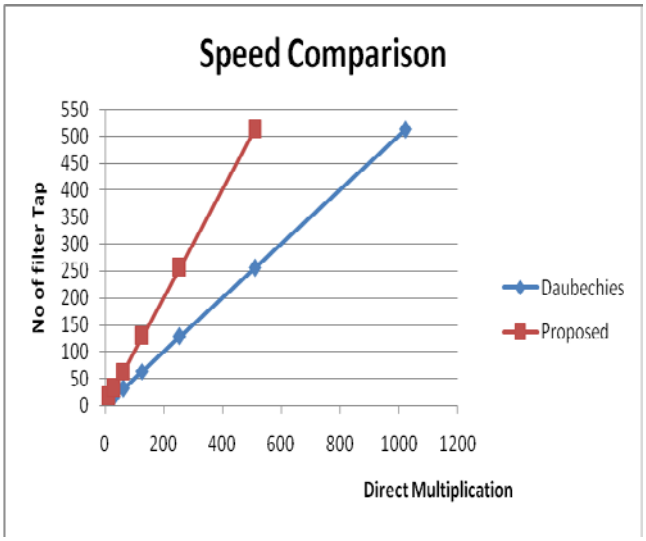

Fig. 9. Speed comparison of two DWT architecture

5. Reconfigurable PEs Array

The entire processing elements within each processor array are similar in design. Each processing element consists of Random access memory (RAM) block, Address generator block, Multiplier and Adder/subtracted block, RAM block is used to store the input data to the processing element. Second memory is used to store input data, this data added or subtracted with the multiplier output. There are two address generators. The first is used for supplying read addresses to the RAM block internal to the PEs. The second is used for supplying write addresses for the data that exit the PEs showed in figure 10. The addressing scheme is same for both address generators. The data path can be dynamically reconfigured as using configurable bit stream.

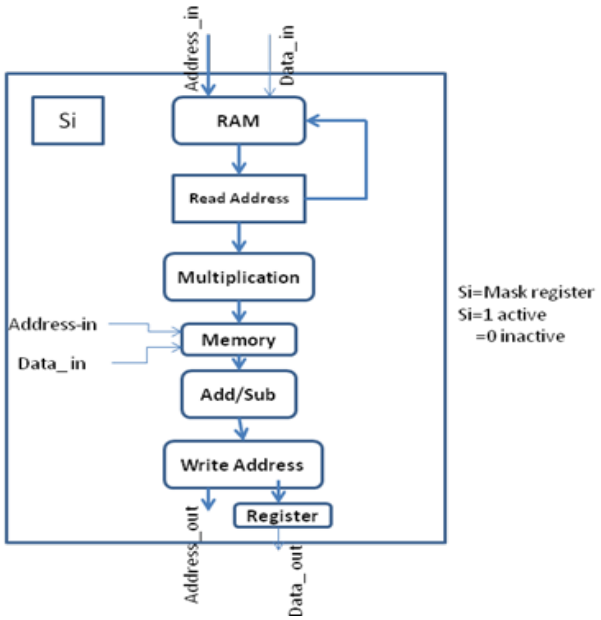

Fig. 10. Basic structure of processing element(PE)

IJSER

6. Architecture of Novel Reconfigurable Digital Signal Processor

The architecture makes use of some building blocks like processing elements (PEs).Implementing all these blocks on LUT based platforms for their dynamic reconfiguration depending on the algorithm to be realized, becomes very expensive with respect to power consumption. So, the functional building blocks (PE) are made fixed in hardware and a reconfigurable switching matrix has been incorporated in order to establish connections among them for implementing a particular algorithm. Thus the width of the configuration bit stream is significantly reduced as the switching matrix only need to be configured for realizing a given function which is turn reduced the size of the configuration memory. The bit stream for configuring the switching matrix depending on a particular function is stored in configuration memory which is generally flash memory.

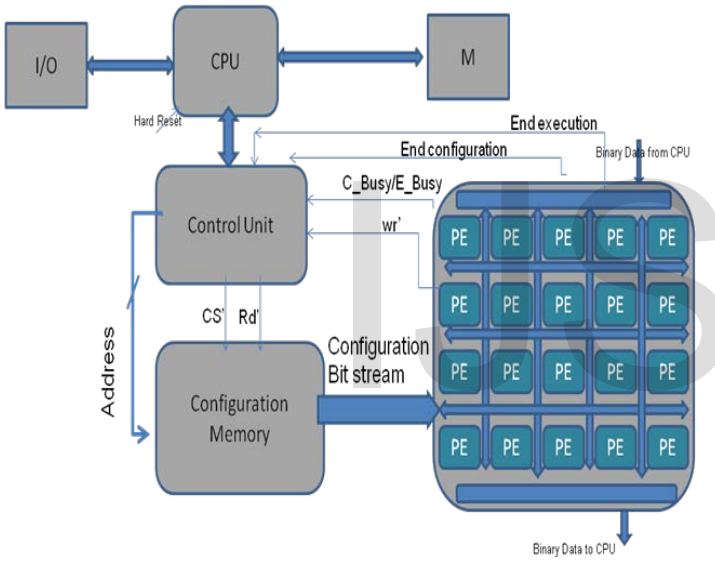

Fig. 11. Architecture of a reconfigurable processor

7 Experimentation and Results

The multiplier unit of processing element described in this paper has been implimented by us.This being heart of the entire system .The multiplier unit of the system has been design to multiply two number.The code for the circuit is written in verilog using XILINX ISE 9.1i version.The multiplier unit of the system is implimented and tested on FPGA board for proper working.Wide range of input combination is given and the output has been verified.

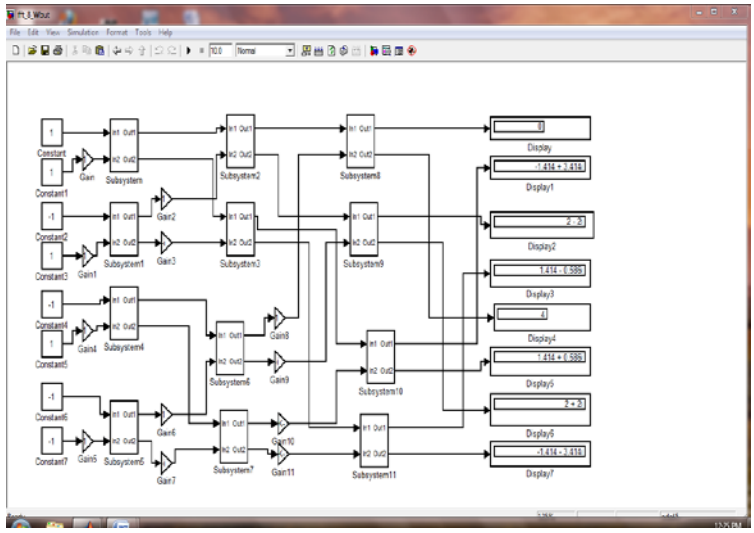

Fig. 12. Basic structure of processing element(PE)

8. Comparative Study of Hardware Utilization on DWT Architecture by Xilinx ISE 9.1i

/Synthesis Result of DWT pipeline architecture

Device utilization summary:

Cell usages :	202
Number of Slices:	57 out of 10752
Number of Slice Flip Flops:	83 out of 21504
Number of 4 input LUTs:	79 out of 21504
Number used as logic:	78
Number used as Shift registers:	1
Number of IOs:	28
Number of bonded IOBs:	28 out of 448

Timing Summary:

Speed Grade: -10

Minimum period: 2.592ns
Minimum input arrival time before clock: 4.494ns
Maximum output required time after clock: 4.677ns

Speed: 385.840MHz

/Synthesis result of proposed DWT parallel pipeline architecture

Device utilization summary:

Cell usage:	133
Number of Slices:	27 out of 10752

Number of Slice Flip Flops: 2 out of 21504
Number of 4 input LUTs: 45 out of 21504
Number used as logic: 33
Number of IOs: 28
Number of bonded IOBs: 28 out of 448
Number of DSP48s: 1 out of 48

Timing Summary:

Speed Grade: -10

Minimum period: 0.798ns
Minimum input arrival time before clock: 2.404ns

Speed: 1252.662MHz

Power summary:	P(mW)
Total estimated power consumption:	452

8.1 Time Delay Calculation of DWT, Matrix Multiplication and FFT

FFT:
Total Time 13.681ns (12.870ns logic, 0.811ns route)
(94.1% logic, 5.9% route)

Matrix Multiplication:
Total Time 9.893ns (9.348ns logic, 0.545ns route)
(94.5% logic, 5.5% route)

DWT:
Total Time 14.893ns (12.208ns logic, 2.685ns route)
(82.0% logic, 18.0% route)

9 Conclusion

In this paper we have proposed a novel reconfigurable architecture which performed DWT of N-sample sequence in only N/2 clock cycles.This result allows high speed and it has been achived by means parallel pipeling.Hence , the proposed architecture can be applied in image transmission in wireless network as well as digital signal processing which required high speed processing. Proposed parallel based matrix multiplication architecture which increase the speed of computation and it is reconfigurable with the need of specific application. When the proposed pipeline FFT architecture the PEs arrays are reconfigured,the other PEs arrays are computing one step of FFT. So,it give the higher speed on computation as well as the hardware complexity is reduced. The computational complexity analysis of FFT proved that it is better than the equivalent DFT. The use of functional building blocks(PEs) in fixed hardware for performing the DSP computations increases performance,while retaining much of the flexibility of a software solution by incorporating a reconfigurable switching matrix in order to configure connectivity among the blocks for a specific application. Thus it can be concluded that the proposed reconfigurable DSP processor can provide higher performance in terms of speed of execution.

Acknowledgment

I would like to thank Dr. Amitabha Sinha for given the innovative idea.

References

[1] P PavelSinha, AmitabhaSinha, Dhruba Basu ,"A Noval Architecture of a Reconfigurable Parallel DSP Processor " proc. The 3rd Int'1 IEEE Northwest, Workshop on circuits and system .

[2] John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing Principles, Algorithims Applications", Third Edition, PrenticeHallofIndiaPrivateLimited,NewDelhi,2005(©1996 by Prentice Hall, Inc. Upper Saddle River, New Jersey 07458, U.S.A ISBN 81-203-1129-9).

[3] David S. Taubman and Michael W. Marcellin, JPEG2000: Image Compression Fundamentals, Standards and Practices, Kluwer Academic Publishers, Norwell, Massachusetts, 2002.

[4] Si-J. Chang, M. Ho Lee, and J. Park, "A high speed VLSIarchitecture of discrete wavelet transform for MPEG-4," IEEEProc. Of the Int. Conf. On Cons. El. 97, N.Y. 1997.

[5] Xilinx ,"Vertex-II Platform FPGAs: Complete Data Sheet"(DS031, v3.5, November 5,2007).Available : http://www.xilinx.com

[6] keshab k parthi "VLSIArchitectures for Discrete Wavelet Transforms" , *IEEE Trans. 1993*

[7] Andreas Antoniou" Digital signal processing, signal system and filter" Copyright © 2006 by The McGraw-Hill Companies, ISBN 0-07-145424-1).

[8] John Villasenor, Brad Hutchings, "The Flexibility of Configurable Computing Providing the Hardware for Data-Intensive Real-Time Processing", IEEE Signal Processing Magazine, September, 1998.

[9] Po-Chih Tseng, Chao-Tsung Huang, and Liang-Gee Chen,"RECONFIGURABLE DISCRETE WAVEL.ET TRANSFORM ARCHITECTURE FOR ADVANCED MULTIMEDIA SYSTEMS"IEEE Trans,2003.

[10] Sharbari Benerjee, Amitabha Sinha , "Performance Analysis of Different DSP Algorithms on Microcontroller and FPGA" Proc. Int'1 conf(an IEEE conference)on Advances in Computation tools for Engineering Application,2009.

[11] , R. M. Owens, and M. J. Irwin, "VLSI Architectures for the Discrete Wavelet Transform," *IEEE* Trans. on Circ. and Syst. ***11***, vol. 42, 1995, pp.305-316

[12] M. Vishwanath, R. M. Owens, and M. J. Irwin, "VLSI Architectures for the Discrete Wavelet Transform," *IEEE* Trans. on Circ. and Syst. ***11***, vol. 42, 1995, pp.305-316.

[13] J. Fridman, and **S.** Manolakos, "Discrete Wavelet Transform: Data Dependence Analysis and Synthesis of Distributed Memory and Control Array Architectures," *IEEE* Trans. *On* Sig. Proc., vol. 45, 1997, pp. 1291-1308.

[14] *G.* Knowles, "VLSI Architecture for the Discrete Wavelet Transform," *El.* Lett., vol. 26, 1990, pp. 1184-1 185.

[15] A. Grzeszczak, M. K. Mandal, S. Panchanatan, "VLSI Implementation of Discrete Wavelet Transform," *IEEE* Trans. *on VLSI* Systems, vol. 4, n. 4, 1996, pp. 421-433.

[16] C. Yu, C. H. I Hsieh, and S. J. Chen, "Design and Implementation of

a Highly Efficient VLSI Architecture for Discrete Wavelet Transforms," Proceedings of *IEEE* Int. Con8 *on* Custom Integrated Circ., 1997, pp. 237-240.

[17] K. K. Parhi, and T. Nishitani, "VLSI Architectures for Discrete Wavelet Transforms," *IEEE* Trans. *on* VU1 Systems, vol. 1, n.2, 1993, pp. 191-202.

[18] Nikhil.Ambekar , Rohit.Patil, Rajashekargouda.Patil Subray.Bhat "Fast Matrix Multiplication" IEEE 2006.

[19] A.Singh , A. Mukherjee, M. Sadowska, " Interconnect pipelining in a throughput- intensive FPGA architecture," Proc. ACM/SIGDA Int. Symp. FPGA,Monterey, CA, 2001.

[20] H. A. ElGindy, and Y. L. Shue. "On Sparse Matrix-Vector Multiplication with FPGA-based System", FCCM, Apr 2002.

[21] Y. El-kurdi, W. J. Gross, and D. Giannacopoulos. "Sparse Matrix-Vector Multiplication for Finite Element Method Matrices on FPGAs". *2006 IEEE Symposium on Field-Programmable Custom Computing Machines*, April 2006.

[22] Kinane, A., Muresan, V., O'Connor, N.: Towards an Optimised VLSI Design Algorithm for the Constant Matrix Multiplication Problem. In: Proc. IEEE International Symposium on Circuits and Systems, Kos, Greece (2006)

[23] Zhuo, L., Prasanna, V.K.: Scalable and modular algorithms for floating-point matrix multiplication on reconfigurable computing systems. IEEE Trans. Parallel Distrib. Syst. **18**(4), 433–448 (2007)

[24] Farid. N. Najm 'A Survey of Power Estimation in VLSI Circuits', IEEE Transaction on VLSI, 1994.

[25] S. He and M. Torkelson 'Design and Implementation of a 1024-point Pipeline FFT Processor', IEEE 1998 Custom Integrated Circuits.

[26] E.H. Wold and A.M. Despain. 'Pipeline and Parallel FFT Processors for VLSI Implementations', IEEE Transactions on Computers, vol. C-33, 1984.

[27] Clark D. Thompson 'Fourier Transform in VLSI', IEEE Transactions on Computers, 1973.

[28] S. He and M. Torkelson, "Designing pipeline FFT prcessor for OFDM (de)modulation," in Proc. 1998 URSI International Symposium on Signals, Systems, and Electronics. Conference, September 1998.

[29] J. Lee, J. Lee, M. H.Sunwoo, S. Moh and S. Oh 'A DSP Architecture for High-Speed FFT in OFDM Systems', ETRI Journal, 2002

[30] TZE-YUN SUNG, HSI-CHIN HSIN, LU-TING KO 'Reconfigurable VLSI Architecture for FFT Processor' WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS, Issue 6, Volume 8, June 2009.

[31] , "An Overview Meher,P. Efficient Systolic Implementation of DFT Using a Low-Complexity Convolution-Like Formulation. Circuits and Systems II: Express Briefs, IEEE Trans-actions on 53(8) (Aug. 2006).

[32] Altera White Paper, "FPGA Provide Reconfigurable DSP Solutions", August 2002,ver 1.0(© 2001 Altera Corporation) Available : http://www.altera.com

[33] D.Cronquist, P. Franklin, C. Fisher, M.Figueroa, C.Ebeling, "Architecture design of reconfigurable pipelined datapaths," Proc. 20th Anniversary Conf. Advanced Research VLSI, Atlanta, GA ,1999, pp.23-40.

[34] A.Sinha,A.Karmakar,K.Maiti,P.Halder, "Reconfugurable Parallel Architecture for Signal/Image Processing Applications".Proc. Embedded System Conference , Stuttgart,Germany,Octobor 9th-10th 2001.

IJSER